AuthenTec, Inc.
Personal Security for the Real World™

Dated 10-25-2000

AES-4000 USB (Yukon) Reference Design
Theory of Operation

The AES-4000 USB Reference Design mates the Fingerprint Sensor through a USB port. Using the reference design information, a customer can quickly develop a design to suit their needs. The Theory of Operation below explains the rationale behind components used, implementation and provides a board level understanding of the circuitry.

USB Interface

Connection to the host USB port is accomplished via an attached cable. A standard USB cable has four wires and a shield. They are power, power return, D+ and D- (the D+ and D- are differential data lines that transmit and receive data bidirectionally) and the shield.

The power and power return go through L3 and L4 (ferrite beads) to provide the board with power. These components suppress high frequency emanations on the power and power return that would radiate into the cable. In addition they suppress RF and burst signals that may come into the board. These components should be less than 0.1 ohm DC resistance. They should have less than 100 ohms impedance at 12MHz. These ferrite beads are specified to be 220 ohm at 100MHz.

The shield is connected directly to the board ground. This configuration has proven to minimize the amount the emanations as found during compliance testing. With the combination of L3, L4 and the shield termination to board ground, this design was compliant to EN55022 and IEC/EN 1000/61000-4-3.

R16 and R17 provide for series termination of the USB data lines. This design is compliant when using 24 ohms.

C34 and C35 provide edge rate compliance on the USB waveforms, when needed. This particular reference design does not need them since the length of cable that AuthenTec has standardized upon for evaluation units is 1 meter. The 1 meter cable has inherent capacitance that eliminates the need for C34 and C35 in this implementation. Shorter cables or deployment within other configurations or embedding the unit may require these components to be USB compliant.

U6 provides ESD suppression on the USB data and power lines. This component supports compliance with IEC/EN 1000/61000-4-2 for the USB interface portion of the design. The power and power return connection should be on the USB side of the ferrite beads, L3 and L4, since the purpose of this component is to suppress attacks from the USB cable/interface. Steering diodes within U6 provide bipolar suppression to a clamping zener within the device. The power content from the event is dissipated within U6, and is not simply directed to the positive or negative rail. The capacitance of the connections to the data lines that U6

exhibits should be less than or equal to 15 pf. The connections to the data lines should be on the side of the series termination resistors closest to the onboard USB transceivers (within the AuthenTec sensor).

R15 provides the D+ pullup to 3.3V to identify this module as a high speed node. Note that the USB specification calls for an *equivalent* impedance of 1500 ohms to 3.3V. Therefore, termination to other voltages via a proper impedance to create this equivalence is an option

The transceivers and all other elements required to implement the USB interface are contained within the AuthenTec AES4000 sensor. The connections are on pins 71 and 72.

Power Management Interfaces

After power and power return is routed through L3 and L4, power filtering is accomplished with C1 and C2.

Current Sense & Cutoff Switch

C25 provides the additional filtering that is recommended by the supplier of U5. It should be located physically and electrically close to the input of U5. C33 provides bypassing for U4. If C1 and C2 are located close enough to U5 and U4, C25 and C33 may be omitted.

R11 sets the current limit for U5. The formula for the resistance of R11 is $1380/I_{limit}$. So, 7.5K equals a set current of 184mA. 10K would equal 138mA. R11 should have a 1% tolerance.

U5 functions to limit current over a programmable threshold. It provides a fail-safe safety function to limit current into the AES4000, so that it will not heat up beyond a preset limit, regardless of any failure.

The function of U4 is to recognize the over-current condition and to cycle power via ON-OFF commands to U5. The time period when the command to U5 is OFF is approximately 66 milliseconds.

AES4000 Analog Power Switch

C4 provides the bulk capacitance for storage when Q1 turns on the 5V_array power. C4 should be located close to the input of the FET, Q1. R7 provides gate level bias to keep the FET off when the FPS_PWR signal has not actively pulled the signal line low. C11 should be located close by the "output" of Q1.

Power Rail Bypassing

C5, C6, C7 and C8 provide the bypassing for the digital power rail (5V) that goes to the AES4000. Each of these capacitors should be located next to a power and power return pin at each side of the sensor. They should be connected to those pins without going through a via.

C12, C13, C14 and C15 provide the bypassing for the analog power rail (5Varray) that goes to the AES4000. Each of these capacitors should be located next to a power and power return pin at each side of the sensor (as applicable). They should be connected to those pins without going through a via.

C36 provides DC filtering on the 3.3V regulator output. It is needed for stability of the regulator. A value of 4.7uF reduces the ripple of the 3.3V rail to a satisfactory amount. Too much noise on this power rail can affect the integrity of data transmission via the voltage thresholds for the transmitters of the AuthenTec sensor USB interface.

Power Distribution

Power and power return should be layered and routed close to each other so that power capacitance is maximized. Wherever and whenever possible low impedance paths (wide and short) should be used.

Sensor Interfaces (not already discussed)

When placing the sensor, pin one should face down and lower right corner (as the finger approaches), close to the knuckle and away from the fingertip. This is done to minimize the time the dynamic optimization circuit takes to optimize the register values. FingerLoc begins scanning from the pin one side of the sensor. If this is located at the bottom of the finger, more information is available for the optimization circuits to work quickly. Please refer to the product specification for explanation of fingerprint acquisition.

Clock
C19, C21, R10 and Y1 provide a crystal based oscillator circuit for the operation of the AES4000. Normal precautions, such as ground shielding, during PWB layout to minimize emanations from this circuit should be implemented.

USB Configuration ROM
The interface to the USB configuration ROM is via 4 lines to U3. This ROM would be needed for customers that will have a different VID and PID for the USB enumeration. The reference design as shipped from AuthenTec will not have this device populated, since the VID and PID for AuthenTec is pre-programmed on board the AES4000. R8 provides a ncessary pullup when the ROM is absent. The AES4000 will detect the absence of data from the ROM (all high) and will not initiate any data transfer. C16, which provides bypassing, is not populated when U3 is absent.

Charge Pump Filter
R9, C17, C20 provide the filtering circuit for the internal PLL (phase lock loop). Since the PLL_BYPASS is NOT active in this configuration (pin 33), these components are needed. If the PLL_BYPASS were active (high) these components do not need to be populated.

Reset
C18 provides the capacitance to ramp up after the rise of the rail. From when the voltage rail reaches operational range, the reset circuit delays this voltage at this node so that the sensor will be properly reset. The AES4000 has an internal resistance, approximately 50K, that provides the RC circuit for the reset function, in conjunction with C18.

1.2V Reference
A stable 1.2V reference is required for the 3.3V regulator operation. To enable the external reference, the VREF_EN input must be high. Operating current from the sensor is approximately 100uA. A 3% tolerance for this component is acceptable.

FDRV (finger ring drive node)
The AES4000 utilizes the finger ring to detect and analyze a candidate finger/fingerprint. C23 and C24 are split to support improved ESD immunity. A value of 27pF on each capacitor provides the recommended capacitance for the finger detect auto-calibration.

ESD Protection (from finger ring drive node, FDRV, to FingerRing)
R14 provides a series resistance for the ESD pulse to be mitigated. It is low enough in resistance to minimize the attenuation of the FDRV signal yet assist in ESD immunity.

C22 provides AC coupling of the FDRV signal to the finger ring.

L2 provides a high frequency series inductance to mitigate the ESD pulse high frequency characteristics.

U9 provides fast clamping action on the finger ring node. Typically, with PWB assemblies that have proper layout, ESD pulses can be successfully clamped at less than 30V. The loading effect of U9 should be less than 15pF. Additional capacitive loading will adversely affect the sensitivity of the AES4000 to recognize and analyze fingers. U9 should be connected to the power rails immediately surrounding the AES4000. This is presuming an ESD attack from the sensor interface. U9 provides ESD suppression on the finger ring and local power lines. This component supports compliance with IEC/EN 1000/61000-4-2 level 4 for the sensor interface portion of the design.

Layout and routing of this node is important to minimize the capacitive and inductive effects of the PWB. Short traces and close placement with a minimum of via holes from U9 to the finger-ring will be important to minimize the impact of ESD events.